a first contact to said actual gate; and

a second contact to said conductive portion of said spacer at said pseudo gate, wherein said first actual gate and said second ~~actual~~ gates cooperate to operate a single transistor.

24-32 (Canceled).

33. (Currently amended) A transistor device having multiple gates comprising:

a first source/drain region formed in a semiconductor substrate;

a second source/drain region formed in said semiconductor substrate spaced from said first source/drain region;

a gate structure including a first oxide layer formed between said first and second source/drain regions defining a first gate of a transistor;

a secondary oxide layer formed over at least a portion of said gate structure;

a spacer formed over at least a portion of said gate structure and said second oxide layer, at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate of said transistor and at least a second portion of said spacer positioned over said conductive portion of said spacer, wherein said second portion of said spacer is nonconductive;

a first contact to said gate structure; and

at least a second contact to said conductive portion of said spacer wherein said first and second gates cooperate to operate said single transistor ~~by affecting said first and second source/drain regions~~.

REMARKS

Claims 15-19, 23 and 33 were presented for examination. Claims 15-19, 23 and 33 were rejected. Claims 15, 17-18, 23 and 33 have been amended.

Rejections Under 35 U.S.C. § 112

Claim 33 was rejected under 35 U.S.C. § 112, first and second paragraph as being unclear and for not being adequately described in the specification. Claim 33 has been amended to delete the unclear phrase, "by affecting said first and second source/drain regions." However, the Applicants respectfully disagree that "source/drain" regions are not clearly identified in the specification. Gated transistors with spacers are well-known by those skilled in the art to include source/drain regions. Additionally, the source/drain regions appear in Figs. 3, 8, 10, and 12. Applicants believe that claim 33 is no longer unclear and is adequately supported by the specification. Applicants request that the Examiner withdraw his rejection to claim 33.

Claim 23 was rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 23 has been amended to provide antecedent basis for the indicated subject matter. Applicants believe that claim 23 is now in compliance with 35 U.S.C. § 112, second paragraph and request that the Examiner withdraw his rejection to claim 23.

Rejections Under 35 U.S.C. § 102(b)

Claims 15, 17, 19, 23 and 33 were rejected under 35 U.S.C. § 102(b) as being anticipated by Rao '139. Applicants respectfully traverse.

Claims 15, 17, 19, 23 and 33 were amended to include the limitation of a second portion of a spacer that is nonconductive and positioned over a conductive portion of the spacer. Support for this limitation can be found in the specification on page 10, lines 14-26, and as element 154 in Figures 7- 8

Claim 15, as amended, recites, in part, a multiple gate transistor structure comprised of a gate, a conductive spacer positioned under a nonconductive spacer that acts as a second gate and two contacts, one connected to the gate and a second connected to the conductive space. All the elements cooperate to operate as a single transistor.

Rao '139 discloses a semiconductor structure with two adjacent single gated transistors sharing a common source/drain region and have overlapping gates. This is in contrast to the claimed invention which discloses having only one transistor comprised of multiple gates. Therefore, Rao '139 fails to disclose the limitation of a ***single*** transistor with multiple gates. Additionally, Rao '139 fails to disclose either a conductive or a ***nonconductive*** spacer, both of which are presently claimed. Consequently, Applicants assert that not all of the elements of claim 15 are shown or suggested by Rao '139. Therefore, Applicants believe the rejection is unsupported by the art and request that the Examiner withdraw the rejection to claim 15.

Independent claims 17, 19, 23, and 33 as amended, also recite a single multiple gated transistor with both conductive and nonconductive spacers. Consequently, for the same reasons discussed above with respect to claim 15, Applicants assert that not all of the elements of claims 17, 19, 23, and 33 are shown or suggested by Rao '139. Therefore, Applicants believe the rejection is unsupported by the art and request that the Examiner withdraw the rejection to claims 17, 19, 23, and 33.

Claims 15-19, 23 and 33 were rejected under 35 U.S.C. § 102(b) as being anticipated by Rao '263. Applicants respectfully traverse.

Rao '263 recites a semiconductor structure with a plurality of adjacent single gated transistors sharing a common source/drain region and have overlapping gates. However, Rao '263 fails to teach a multiple gated structure cooperating to operate as a ***single*** transistor with both conductive and ***nonconductive*** spacers as recited in claim 15. Consequently, Applicants also assert that not all of the elements of claim 15 are shown or suggested by Rao '263. Therefore, Applicants believe the rejection is unsupported by the art and request that the Examiner withdraw the rejection to claim 15.

Independent claims 17, 19, 23, and 33 as amended, also recite a single multiple gated transistor with conductive and nonconductive spacers. Consequently, for the same reasons discussed above with respect to claim 15, Applicants also assert that not all of the elements of claims 17, 19, 23, and 33 are shown or suggested by Rao '263. Therefore, Applicants believe the rejection is unsupported by the art and request that the Examiner withdraw the rejection to claims 17, 19, 23, and 33.

Claim 16 depends from independent claim 15 and is patentable for the same reasons as claim 15. Additionally, claim 16 recites further limitations not shown or suggested by the prior art. For example, claim 16 also recites a conductive spacer which, as mentioned above, is not taught in Rao '263. Therefore, Applicants believe the rejection of claim 16 is unsupported by the art and request that the Examiner withdraw the rejection to claim 16.

CONCLUSION

For the above reasons, Applicants respectfully submit that the above claims as amended recite allowable subject matter. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
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